Register for Certification exam

Thank you for taking the Week 6 : Assignment 6.

Week 6 : Assignment 6

Your last recorded submission was on 2021-09-06, 16:09 IST

Due date: 2021-09-08, 23:59 IST.

1) Which of the following statement(s) is/are true? *1 point*

a. Organizing memory in multiple levels may result in faster data access.
b. As we move away from the processor the speed of memory increase.
c. By keeping commonly used data in the memory that is near to processor, memory access time may increase.
d. None of these.

- [x] a.
- [ ] b.
- [ ] c.
- [ ] d.

2) Consider a three-level memory hierarchy (cache - main memory - magnetic disk). Which of the following interfaces of the memory hierarchy is/are managed by operating system? *1 point*

a. Cache – magnetic disk
b. Cache - Main memory
c. Main memory - magnetic disk
d. None of these.

- [ ] a.
- [ ] b.
- [x] c.
- [ ] d.

3) Consider a machine which takes 2 nanosecond to fulfill a read request for cache hit and 45 nanoseconds to fulfill a read request for cache miss. If a program results in 90% of cache hit then the average read access time will be _____ nanoseconds.

6.3

1 point

4) Consider a 2-level memory hierarchy consisting of a single-level cache memory and the main memory. The access times for the cache memory and main memory are 10 nanoseconds and 100 nanoseconds respectively. If a program is using cache for 85% of the time. The speedup gain by using cache will be _____.

4.25

1 point

5) Consider a main memory with 1024 blocks with block size of 32-bit each and a cache memory which consist of 128 blocks. If we use direct mapping then block 128 and 256 will be mapped to which blocks of cache memory?

1 point

a. 128,256
b. 0, 0
c. 1, 1
d. 0, 1

- ○ a.
- ◉ b.
- ○ c.
- ○ d.

6) Consider a set-associative cache that consists of 256 blocks divided into 16-block sets and a byte addressable main memory of size 512Kbytes, with block size of 32 bytes each. How many bits will be there in the TAG, SET and WORD fields respectively? *1 point*

a. 10, 4, 5
b. 10, 5, 4
c. 10, 5, 5
d. 10, 4, 4

- (●) a.
- ( ) b.
- ( ) c.
- ( ) d.

7) A computer has 4 Gbyte memory with 32-bit words, where the computer uses word-level addressing. Each block of memory stores 64 words. The computer has a direct-mapped cache of 128 blocks. How many bits will be there in the TAG field? *1 point*

a. **16**
b. **17**
c. **18**
d. **19**

- ( ) a.
- ( ) b.
- ( ) c.
- (●) d.

8) Consider an N-way set associative memory? What will happen if we increase value of N? *1 point*

a. Search time in cache will increase.
b. Freedom of mapping main memory block into cache will increase.
c. Size of set will increase.

- [x] a.
- [x] b.
- [x] c.

9) Consider a processor with an average CPI of 1.5, which runs a program with the following instruction mix: ALU instructions – 50%, LOAD – 25%, STORE – 10%, BRANCH – 15%. Assume that the cache miss rate is 5%, and the miss penalty is 33 cycles. What will be the effective CPI for a unified L1-cache, using write back and write allocate, assuming that the probability that the cache is dirty is 10%. *1 point*

a. 1.35
b. 1.85
c. 2.45
d. 3.95

- ○ a.
- ○ b.
- ○ c.
- ◉ d.

10) Which of the following approaches can be used for reducing cache miss rate? *1 point*

a. Use larger block size
b. Use larger cache
c. Use higher associativity

- ☑ a.
- ☑ b.
- ☑ c.

You may submit any number of times before the due date. The final submission will be considered for grading.

Submit Answers

Note: All these answers are confirmed from our side, we don't guarantee that you will get a 100% score. These are our own answers that we are sharing with you all. If you have any doubt that our answers are not correct then feel free to discuss (in-group) or do your answer.

Most important: We don't promote any type of cheating, these answers are only for those students who are not able to do it on their own or need some help.